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15. (Amended) A semiconductor device having at least two levels of interconnecting metallurgy, said semiconductor device comprising:

a first level of substantially silicide free metallurgy; and

an uppermost layer of metallurgy including a bonding pad, wherein a top of said uppermost layer comprises a silicided surface,

wherein a thickness of said uppermost layer reduces sensitivity to resistivity shifts associated with said silicided surface.

21. (Amended) A semiconductor device comprising:

an exterior surface having a top level of metallurgy,

wherein an exposed portion of said top level of metallurgy comprises a bonding pad,

wherein an upper 10% to 20% of said bonding pad comprises a silicided surface, and

wherein a thickness of said uppermost layer reduces sensitivity to resistivity shifts associated with said silicided surface.

29. (Amended) A semiconductor chip comprising:

an exterior surface having a top level of metallurgy; and

an interior having at least one internal level of metallurgy,

wherein said top level of metallurgy is thicker than said internal level of metallurgy,

wherein an exposed portion of said top level of metallurgy comprises a bonding pad,

wherein an upper 10% to 20% of said bonding pad comprises a silicided surface, and

wherein a thickness of said uppermost layer reduces sensitivity to resistivity shifts associated with said silicided surface.